System and Method for Refreshing a Dynamic Memory Device

ABSTRACT

A memory device (10) includes an array (12) of memory cells arranged in rows and columns. Preferably, each memory cell includes a pass transistor coupled to a storage capacitor. A row decoder (18) is coupled to rows of memory cells while a column decoder (14) is coupled to columns of the memory cells. A refresh controller (19) is adapted to generate memory cell addresses for array (12) during a refresh sequence. In a preferred embodiment of the present invention, the refresh controller ensures that no shared sense amplifiers (24) are activated during consecutive refresh cycles, allowing a portion or all of the time required for precharging the bitlines to be saved. In a preferred embodiment, consecutive refresh cycles can be located closer together in time because a second refresh cycle may be initiated prior to the completion of a first refresh cycle.